AMENDMENTS TO THE CLAIMS

Please cancel claims 7 and 29 without prejudice.

1. (CANCELED)

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 21, wherein said apparatus comprises a plurality of bits each configured to evenly load said input groups.

3. (CANCELED)

4. (CANCELED)

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said bits comprise programmable interconnect matrix (PIM) bits.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 21, wherein said apparatus is configured to provide flexible reprogramming of said first programmable interconnect matrix and second programmable interconnect matrix.

7. (CANCELED)

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein a configuration of said apparatus is expandable in a horizontal direction.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 8, wherein said configuration of said apparatus is expandable in a vertical direction.

10. (ORIGINAL) The apparatus according to claim 9, wherein said configuration reduces complexity of physical routes of said distributed input groups.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 21, wherein a layout of said apparatus is deterministic.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 21, wherein a delay of said apparatus is deterministic.

13. (CANCELED)

14. (CANCELED)

15. (CANCELED)

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)

21. (CURRENTLY AMENDED) An apparatus comprising:

a first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order and (ii) present said distributed input group of signals in a second order; and

a second programmable interconnect matrix having one or more second multiplexers configured to receive said distributed input group of signals from said first programmable interconnect matrix in said second order, wherein (i) said first order of said signals are different from said second order of said signals, ~~and~~ (ii) said second order of said signals are disposed in an input-re-order channel and (iii) said apparatus is scalable.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 21, wherein said distributed input group of signals are divided into a first group of input signals and a second group of input signals, wherein said first group of input signals is presented to one of said first multiplexers and said second group of input signals is presented to another of said first multiplexers.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 22, wherein any one of said second multiplexers is configured to receive a mix of inputs from said first and second groups of input signals.

24. (CURRENTLY AMENDED) An apparatus comprising:

a first distributed multiplexer configured to generate a first output signal in response to (i) a first portion coupled to a first group of input signals and (ii) a second portion coupled to a second group of input signals; and

a second distributed multiplexer configured to generate a second output signal in response to a (i) a first portion coupled to a third group of input signals and (ii) a second portion coupled to a fourth group of input signals, wherein (i) said first portion of said first distributed multiplexer is physically separated from said second portion of said first distributed multiplexer on a

layout area, ~~and~~ (ii) said first portion of said second distributed multiplexer is physically separated from said second portion of said second distributed multiplexer on said layout area, and (iii) said apparatus provides (a) a deterministic layout area and (b) an input grouping configuration which allows said first and second groups of input signals to remain consistent across any number of distributed multiplexers.

25. (PREVIOUSLY PRESENTED) The apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer comprises a programmable multiplexer bit coupled to any of said first group of input signals and (ii) said second portion of said first distributed multiplexer comprises a programmable multiplexer bit coupled to any of said second group of input signals to allow any of said first or second groups of input signals to pass through on said first output signal.

26. (PREVIOUSLY PRESENTED) The apparatus according to claim 24, wherein (i) said first portion of said second distributed multiplexer and comprises a programmable multiplexer bit coupled to any of said third group of input signals and (ii) said second portion of said second distributed multiplexer comprises a programmable multiplexer bit coupled to any of said fourth group of

input signals to allow any of said third or fourth groups of input signals to pass through on said second output signal.

27. (PREVIOUSLY PRESENTED) The apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer is separated from said second portion of said first distributed multiplexer on a die and (ii) said first portion of said second distributed multiplexer is separated from said second portion of second distributed multiplexer on a die.

28. (PREVIOUSLY PRESENTED) The apparatus according to claim 24, further comprising a programmable interconnect matrix configured to be expanded or contracted to implement any number of distributed multiplexers.

29. (CANCELED)

30. (PREVIOUSLY PRESENTED) The apparatus according to claim 24, wherein a plurality of said first distributed multiplexers and a plurality of said second distributed multiplexers are implemented as a programmable interconnect matrix.

31. (NEW) An apparatus comprising:

a first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order and (ii) present said distributed input group of signals in a second order; and

a second programmable interconnect matrix having one or more second multiplexers configured to receive said distributed input group of signals from said first programmable interconnect matrix in said second order, wherein (i) said first order of said signals are different from said second order of said signals, (ii) said second order of said signals are disposed in an input-re-order channel and (iii) said apparatus is configured to provide flexible reprogramming of said first programmable interconnect matrix and second programmable interconnect matrix.